



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

11.07

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/517,877      | 08/12/2005  | Osamu Goto           | 075834.00402        | 1760             |

33448 7590 04/04/2007  
ROBERT J. DEPKE  
LEWIS T. STEADMAN  
ROCKEY, DEPKE, LYONS AND KITZINGER, LLC  
SUITE 5450 SEARS TOWER  
CHICAGO, IL 60606-6306

|          |
|----------|
| EXAMINER |
|----------|

TRAN, THANH Y

|          |              |
|----------|--------------|
| ART UNIT | PAPER NUMBER |
|----------|--------------|

2822

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE  | DELIVERY MODE |
|--|------------|---------------|
| 3 MONTHS                               | 04/04/2007 | PAPER         |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/517,877

Applicant(s)

GOTO ET AL.

Examiner

Thanh Y. Tran

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/13/04</u> . | 6) <input type="checkbox"/> Other: ____.  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al (U.S. 2002/0030200) in view Takeya et al (U.S. 2002/0064195).

As to claim 1, Yamaguchi discloses in figures 1-2 a GaN-based semiconductor device comprising: a GaN substrate (106) having a low-density defect region (104) and core portions (116) present in said low-density defect region (104) in a periodic planar arrangement in said substrate (106) as a high-density defect region (high-density defect region of 116) passing through substrate (106) (see paragraph [0005]); a multilayer structure of GaN-based compound semiconductor layers (comprising 112, 109, 107) formed on said GaN substrate (106); and an electrode portion (105) having an electrode provided on said multilayer structure (comprising 112, 109, 107) and a pad metal (114) electrically connected to said electrode; said electrode portion (105) being provided on said multilayer structure (comprising 112, 109, 107) in a region (region of 104) except said core portions (116) of said GaN substrate (106) (see figure 1, and paragraph [0005]).

Takeya et al discloses in figure 7 a GaN-based semiconductor device, wherein a pad metal (19) formed on an insulating film (20) deposited on an electrode (22) and electrically

Art Unit: 2822

connected through an opening of the insulating film (20) to the electrode (22). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the GaN-based semiconductor device of Yamaguchi by including an insulating film as taught by Takeya et al for protecting the surface of the GaN-based semiconductor device.

As to claim 2, Yamaguchi does not disclose the periodic planar arrangement includes a continuous belt-shaped arrangement, an intermittent belt-shaped arrangement, and a dotted dispersive arrangement. However, Appellants have presented no argument which convinces us that the particular configuration of the core portion is significant or is anything more than one of numerous configurations a person of ordinary skill in the art would find obvious for reducing the dislocation density of the active layer. See *Graham v. John Deere Co.*, 383 U.S. 1,148 USPQ 459.

As to claim 3, Yamaguchi discloses in figures 1-2 a GaN-based semiconductor device, wherein said electrode portion (105) is provided on said multilayer structure (comprising 112, 109, 107) in said low-density defect region (104) between said core portions (116) adjacent to each other.

As to claims 4 and 5, Yamaguchi discloses in figures 1-2 a GaN-based semiconductor device, wherein said pad metal (114) is provided on said multilayer structure (comprising 112, 109, 107); and wherein said electrode (105) is provided on said multilayer structure (comprising 112, 109, 107).

Yamaguchi does not disclose a distance of the pad metal from the center of each core portion is 100  $\mu\text{m}$  or more; and a distance of the electrode being spaced apart from the outer edge of each core portion is 50  $\mu\text{m}$  or more. However, *applying a rule of 100  $\mu\text{m}$  or more for a*

*distance of the pad metal from the center of each core portion; and applying a rule of 50  $\mu\text{m}$  or more for a distance of the electrode being spaced apart from the outer edge of each core portion* would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to claim 6, figure 2 of Yamaguchi further discloses a counter electrode (131) to said electrode is provided on the back surface of said GaN substrate (122).

As to claim 7, figure 2 of Yamaguchi further discloses a counter electrode (122, figure 2) to said electrode is provided on said multilayer structure.

As to claim 8, figure 2 of Yamaguchi further discloses both the electrode (132) and the counter electrode (131) are provided on said multilayer structure in said region except said core portions (116) of said GaN substrate (106/122).

As to claim 9, figure 2 of Yamaguchi further discloses an electrode ("p electrode" 105) is a p-side electrode, and a counter electrode (131, figure 2) is the n-type electrode (see paragraph [0017]).

As to claim 10, Yamaguchi discloses in figures 1-2 a GaN-based semiconductor device, wherein said GaN-based semiconductor device comprises a GaN-based semiconductor light

Art Unit: 2822

emitting device including a GaN-based semiconductor laser device and a GaN-based light emitting diode ("laser diode") (see paragraphs [0004] & [0007]).

### ***Conclusion***

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takatani et al (U.S. 7,015,058), Yamaguchi et al (U.S. 6,855,959) disclose relevant prior art to the invention.

### **Contact Information**

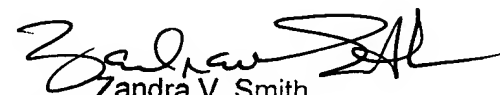
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2822

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

  
Zandra V. Smith  
Supervisory Patent Examiner  
30 March 2007